IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An address generator for generating addresses for testing an addressable circuit, having:

(a) at least one base address register for buffer-storing a base address, the base address register in each case being assigned an associated offset register group having a plurality of offset registers for buffer-storing relative address values;

(b) a first multiplexer circuit, which, in a manner is dependent on a base register selection control signal, switches through an address buffer-stored in the base address register to a first input of an addition circuit and to an address bus, which is connected to the circuit to be tested, wherein the base address register is switched through by the first multiplexer circuit;

(c) a second multiplexer circuit, which, in a manner is dependent on the base register selection control signal, through-connects the offset register group associated with the through-connected base address register to a third multiplexer circuit, which, in a manner is dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group to a second input [[(61)]] of the addition circuit; and

(d) the addition circuit adding the address present at the first input to the relative address value present at the second input to form an address which is buffer-stored in the base address register.

2. (Previously Presented) The address generator as claimed in claim 1, wherein the base address register and the associated offset registers can be initialized by an external test device, via initialization lines.

3. (Previously Presented) The address generator as claimed in claim 1, wherein the address signal switched through to the address bus can be inverted by a controllable inverting circuit.

4. (Previously Presented) The address generator as claimed in claim 1, wherein the number of offset registers of an offset register group is equal to the number of address test jump variants required for testing the circuit.

5. (Previously Presented) The address generator as claimed in claim 1, wherein the circuit to be tested is a synchronous RAM memory with a high operating clock frequency.

6. (Previously Presented) The address generator as claimed in claim 1, wherein the RAM memory has a multiplicity of memory cells which can be addressed via a multidimensional address space (X, Y).

7. (Previously Presented) The address generator as claimed in claim 1, wherein the number of base address registers corresponds to the dimension (d) of the address space of the memory to be tested.

8. (Previously Presented) The address generator as claimed in claim 1, wherein the base register selection control signals and the offset register selection control signals are applied to the address generator by an external test device via an address control signal bus, the bus width of the address control signal bus being less than the bus width of the address bus of the circuit to be tested.

9. (Previously Presented) The address generator as claimed in claim 1, wherein the line lengths of the address bus lines between the address generator and the circuit to be tested are smaller than the line lengths of the address control lines between the test device and the address generator.

10. (Previously Presented) The address generator as claimed in claim 1, wherein the address generator is integrated in the circuit to be tested.